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Publication number:

0 428 005 A2

EUROPEAN PATENT APPLICATION

Application number: 90120787.8

Int. Cl.⁵ G06F 9/26, G06F 11/20

Date of filing: 30.10.90

The title of the invention has been amended
(Guidelines for Examination in the EPO, A-III,
7.3).

Priority: 30.10.89 JP 282164/89

Date of publication of application:
22.05.91 Bulletin 91/21

Designated Contracting States:
DE FR GB

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Microcontroller with non-volatile memory error repair.

An improvement in a microcontroller having non-volatile memory is disclosed. This microcontroller has three types of memory; a ROM (5) in which is recorded a program, a programmable first non-volatile memory (19), and a second non-volatile memory (21) having programmable address data and instruction data zones (21A, 21B). When the result of a detection performed by a comparator (22) shows

that address data sent over an address bus matches address data sent from the address data zone, an instruction data selection section (23) selects and outputs instruction data stored in the instruction data zone corresponding to the address data in the address data zone, instead of outputting instruction data from the ordinary ROM.

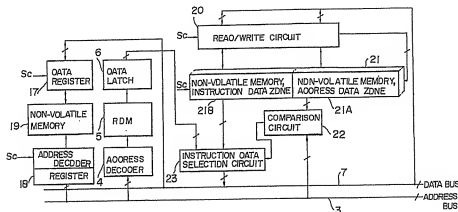


FIG.1

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MICROCONTROLLER

BACKGROUND OF THE INVENTION

The present invention relates to a microcontroller having non-volatile memory.

When a conventional microcontroller having an internal non-volatile memory which is erasable and programmable is activated, an operation notification signal is first sent from a basic signal generation circuit to a program counter. Thereupon, the program counter operates, and an address is sent via an address bus and an address decoder to a ROM in which programs are stored. The instruction at the address in ROM corresponding to that address is then read out from the ROM to an instruction decoder via a data latch and a data bus, and is decoded. A control signal S_c corresponding to the decoded instruction is sent from the instruction decoder to various parts of the microcontroller, and the instruction is executed.

In this conventional microcontroller, programs are recorded in ROM.

The process of developing programs for the above conventional type of microcontroller will now be described with reference to Fig. 6. During the development of a program, the specifications are first verified (step F71), then hardware that satisfies those specifications is selected (step F72). Software is then created in accordance with the selected hardware (step F73), and a program is coded (step F74). After debugging and evaluation of the program (step F75), both hardware and software are checked (step F76). If there is a problem in the software at this point, the flow returns to step F75 for re-verification. Similarly, if there is a hardware problem, and it is determined that the problem cannot be attributed to the software, the flow returns to step F71 for re-verification of the specifications, new hardware is selected, and the above steps are repeated. If there are no problems in the hardware and software, the flow proceeds to the manufacture of samples of the microcontroller (step F77), and the system is evaluated on the basis of those samples (step F78). The process up to the manufacture of microprocessor samples (step F77) must ordinarily be repeated a number of times. If a problem is found during the evaluation of the system containing one of the samples created as described above, the flow must return to step F75. In addition, if a hardware problem is found at this point, the flow must return to step F71 and all of the above steps must be repeated. If no problems are found during system evaluation, mass production and system introduction can start for the first time (step F80).

If, after the sample creation step, the developer finds an error in the program in ROM of a conventional microcontroller created in this way, samples must be manufactured again, no matter how small the correction that is required. This delays the completion of the system, which delays its mass production.

If the programmable ROM is EPROM, the program can be easily corrected, but the package will require a window allowing the passage of ultraviolet light, which will increase the cost of the samples and impede mass production. Note that an alternative method using one-time PROM (in which the program can be written once only, and cannot be erased) could be used, but, as with EPROM, each individual program of a suite of programs must be written individually to ROM, impeding mass production.

Note that, in a conventional microcontroller containing non-volatile memory, all program data could be written to non-volatile memory, and such programs can be corrected. However, the writing of all the programs one-by-one to the non-volatile memory during mass production inevitably increases manufacturing costs.

There is another problem with this type of microcontroller in that, if processing routines of a program stored in ROM, such as, for example, the processing routines shown in Fig. 7, are written to ROM in the sequence in which they are to be processed, the data recorded in ROM can be read out by an external means, making it simple for an unauthorized person to learn the algorithms of the program recorded in ROM.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide a microcontroller which facilitates efficient correction of programs stored in ROM.

Another object of the present invention is to provide a microcontroller which makes it difficult for an unauthorized person to learn the algorithms of programs recorded in ROM.

According to the present invention, there is provided a microcontroller comprising: a ROM in which stores a program; a first non-volatile memory which is erasable and programmable; a second non-volatile memory having erasable and programmable address data and instruction data zones; a read/write means which writes data to the second non-volatile memory and reads data therefrom; a comparison means which compares address data

sent over an address bus and address data sent from the address data zone, and which sends a notification signal if the address data matches; and an instruction data selection means which normally selects and outputs instruction data stored in said ROM but which selects and outputs instruction data stored in said instruction data zone corresponding to the address data in the address data zone if, and only if, the notification signal has been sent out from the comparison means.

If an error is found in a program stored in ROM of the microcontroller of the present invention, a program that corrects the area in which the error was found is first written to a first non-volatile memory. Next, a read/write means is used to write the address of the error area to an address data zone of a second non-volatile memory, and, corresponding to that address, data on an instruction that jumps to the first non-volatile memory is written to a data zone of the second non-volatile memory. When the address of this error area is subsequently called, the address data in the address data zone matches the address data on the address bus, and a notification signal is output from a comparison means. Based on this notification signal, data on an instruction corresponding to the address data in the address data zone, which is stored in the instruction data zone and which jumps to the first non-volatile memory, is selected and output by a selection means, and the corrected program is run.

In this way, if there is an error in the program stored in ROM, the program can be corrected easily and efficiently. This can reduce turn-around time, increase the range of applicable fields, and facilitate upgrading.

In addition, the algorithms of the program can be made difficult to learn from an external means since the processing sequence of the program in ROM is stored in any desired order, and a program that correctly executes the processing sequence is stored in the second non-volatile memory, thus preserving secrecy.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of the structure of the main components of an embodiment of the microcontroller of the present invention, Fig. 2 is a block diagram of the structure of the embodiment of the microcontroller of the present invention, Fig. 3 and Fig. 4 are flow charts used to describe the operation of the microcontroller of the present invention, Fig. 5 is a table used to describe the operation of the present invention, and Fig. 6 and Fig. 7 are flow charts used to describe the operation of a

conventional microcontroller.

DESCRIPTION OF THE PREFERRED EMBODIMENT

A block diagram of the structure of a microcontroller according to the present invention is shown in Fig. 2.

The microcontroller of the present invention comprises a basic signal generation circuit 1; a program counter 2 that outputs to an address bus 3 an address in accordance with a basic signal generated by the basic signal generation circuit 1; address decoders 4, 15, and 18 that decode the address; a RAM 5, a ROM 16, and a non-volatile memory 19 that receive decoder outputs from the decoders; and a data latch 8, a data latch 14, and a data register 17 placed between these memory elements and a data bus 7, to exchange data therebetween. An address decoder 24 is also connected to the address bus 3, and an I/O controller 25 that receives addresses from the address decoder 24 is also connected to the data bus 7.

This embodiment concerns the use of the present invention as a calculation circuit which is also provided with an ALU 11 that performs a calculation using data stored in the RAM 16 or non-volatile memory 19; two registers 9 and 10 that are allocated to the ALU 11 and that receive two data items to be added from the data bus 7; an instruction decoder 8 that gives instructions for the ALU 11 and the two registers 9 and 10 from the data on the data bus 7; and a register 13 connected between the data bus 7 and the address bus 3.

The microcontroller is also provided with a read/write circuit 20, a non-volatile memory 21, a comparison circuit 22, and an instruction data selection circuit 23.

The basic operation of the above embodiment will now be described. When the ALU 11 performs a calculation using data stored in the RAM 16 and the non-volatile memory 19, a control signal S_c is first sent to the address decoder 15 or the address decoder 18 and an address of data stored in the RAM 16 or non-volatile memory 19 is set. Thereupon, the data at the address set in this way is sent from the RAM 16 or the non-volatile memory 19 via the data latch 14 or the data register 17, and the data bus 7, to the register 9 and the register 10. The arithmetic operation is then performed by the ALU 11 in accordance with the decoded instruction, based on the data sent to the register 9 and the register 10.

Note that, during this process, the control signal S_c is sent in accordance with the decoded instruction from the instruction decoder 8 to the

registers 9 and 10 and the ALU 11, and the processing is based on this control signal S_2 . The result of the calculation performed by the ALU 11 is either stored in the register 13, the RAM 16, or the non-volatile memory 19 via an accumulator (hereinafter called "ACC") 12 and the data bus 7, or it is output to the outside via the I/O controller 25.

When execution of the single instruction decoded by the instruction decoder 8 ends, the address output previously from the program counter 2 is incremented by 1, and the resultant address is output. The instruction stored at the address in the ROM 5 corresponding to this new address is sent to the instruction decoder 8, and the instruction is executed as described above.

The operation of the distinctive components of the present invention will now be described with reference to the abbreviated drawing of Fig. 1.

The non-volatile memory 21 has an address data zone 21A and an instruction data zone 21B belonging thereto. The read/write circuit 20 can both write data sent via the data bus 7 to these two zones 21A and 21B, and read data written to the zones.

The comparison circuit 22 compares address data sent from the address zone 21A and address data sent via the address bus 3 and, if the data matches, it sends a notification signal to the instruction data selection circuit 23. The instruction data selection circuit 23 normally transfers instruction data that was recorded in the ROM 5 and has been sent via the data latch 6 via the data bus to the instruction decoder 8, but, if it receives the notification signal from the comparison (in other words, if the address data in the address data zone 21A matches the address data sent via the address bus 3), the instruction data selection circuit 23 transfers data recorded in the instruction data zone 21B of the non-volatile memory 21 to the instruction decoder 8 via the address bus 3. The instruction decoder 8 decodes the instruction data transferred in this way and the instruction is executed.

In the non-volatile memory 19 of this embodiment of the present invention, both data and program instructions can be written to the non-volatile memory 19. Therefore, if program instructions are written to the non-volatile memory 19 and the flow is written in such a manner that instruction data stored in the instruction data zone 21B of the non-volatile memory 21 jumps to a region in the non-volatile memory 19 when the address data stored in the address data zone 21A of the non-volatile memory 21 matches the address data sent via the address bus 3, program data created in the ROM 5 can be easily corrected even after the microcontroller has been manufactured.

The process of developing a system using the

microcontroller of this embodiment will now be described with reference to Fig. 3. From a comparison of Fig. 3 and Fig. 6, it can be seen that the process is the same as the conventional process up to the manufacture of samples. The process differs from the conventional process in that, if a software error is found during the system evaluation of steps F37 and F38, the address of the area containing the error in the software is written to the address data zone 21A of the non-volatile memory 21, an instruction to jump to any desired address in the non-volatile memory 19 is written to the instruction data zone 21B belonging to this address data zone 21A, and the software is corrected in the non-volatile memory 19 (step F40 of Fig. 3). This correction method obviates the need for re-correcting the ROM to correct the samples, so that, by just writing correction areas and additional program data to the non-volatile memories 19 and 21, system introduction and mass production are facilitated.

In addition, if the algorithms of the program shown in Fig. 7 are written to ROM non-sequentially as shown in Fig. 4, to create the commercial product, and data relating the algorithms to each other is written to the address data zone 21A and instruction data zone 21B of the non-volatile memory 21 as shown in Fig. 5, the sequence in which the microcontroller in this embodiment executes the processing routines will be the same as the flow shown in Fig. 7. If this embodiment is organized in this way, the program data in the ROM 5 can be broken up and re-arranged in any desired manner, preventing the use of external means to learn the algorithms of the program written to the ROM 5.

Claims

1. A microcontroller comprising
 - a ROM (5) in which stores a program and
 - a first non-volatile memory (19) which is erasable and programmable; characterized in that said microcontroller further comprises:
 - a second non-volatile memory (21) having erasable and programmable address data and instruction data zones;
 - a read/write means (20) which writes data to said second non-volatile memory and reads data therefrom;
 - a comparison means (22) which compares address data sent over an address bus and address data sent from said address data zone, and which sends a notification signal if said address data matches; and
 - an instruction data selection means (23) which normally selects and outputs instruction data stored in

said ROM but which selects and outputs instruction data stored in said instruction data zone corresponding to said address data in said address data zone if, and only if, said notification signal has been sent out from said comparison means.

2. A microcontroller according to claim 1, wherein, in said second non-volatile memory, an address after an address at which processing ends is stored in said address data zone, and the contents of the next instruction to be executed are stored in said instruction data zone.

3. A microcontroller according to claim 2, wherein instruction data for said program is stored in said ROM in a sequence different from the sequence in which said program is to be executed.

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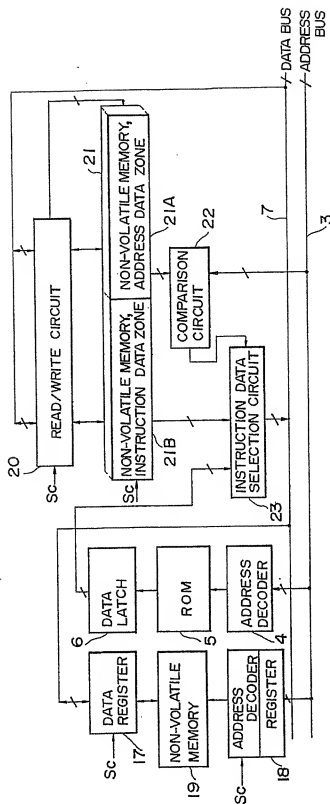


FIG. 1

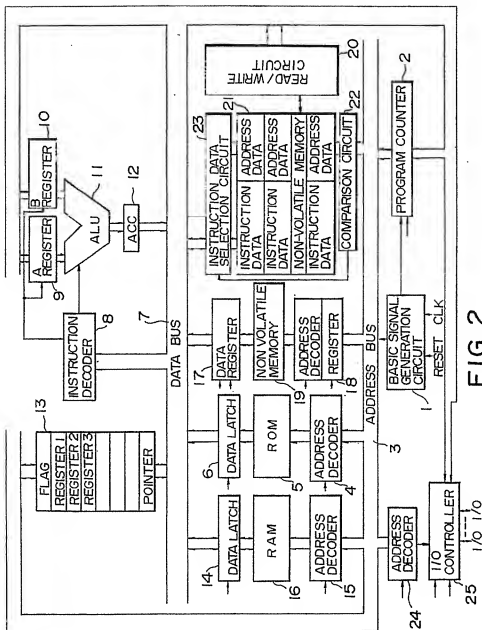


FIG. 2

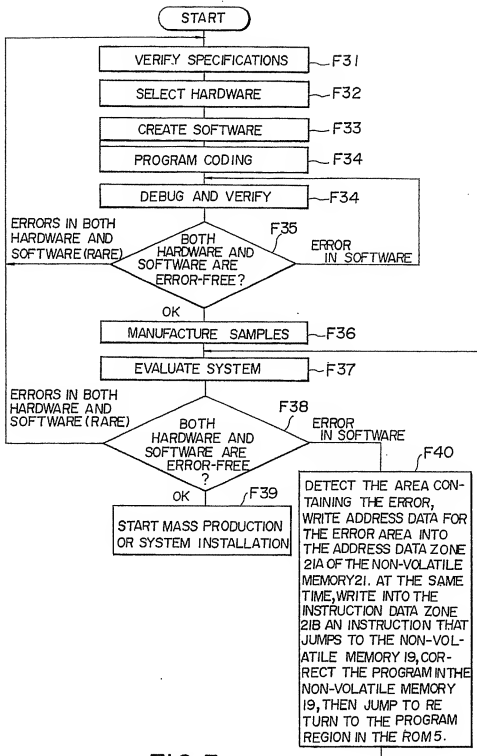


FIG.3

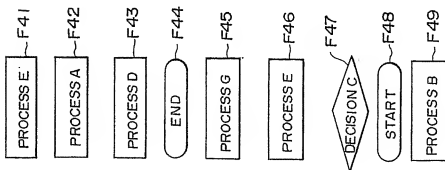


FIG. 4

DATA WRITTEN TO INSTRUCTION DATA ZONE 21B	DATA WRITTEN TO ADDRESS DATA ZONE 21A
JUMP INSTRUCTION TO START PROCESSING	ADDRESS DATA 0
JUMP INSTRUCTION TO PROCESS A	ADDRESS DATA FOR PROCESS AFTER START PROCESSING
JUMP INSTRUCTION TO PROCESS B	ADDRESS OF NEXT PROCESS AFTER PROCESS A
JUMP INSTRUCTION TO PROCESS C	ADDRESS OF NEXT PROCESS AFTER PROCESS B
JUMP INSTRUCTION TO PROCESS D	ADDRESS OF NEXT PROCESS AFTER PROCESS C
JUMP INSTRUCTION TO PROCESS E	ADDRESS OF NEXT PROCESS AFTER PROCESS D
JUMP INSTRUCTION TO PROCESS F	ADDRESS OF NEXT PROCESS AFTER PROCESS E
JUMP INSTRUCTION TO END PROCESSING	ADDRESS OF NEXT PROCESS AFTER PROCESS F

FIG. 5

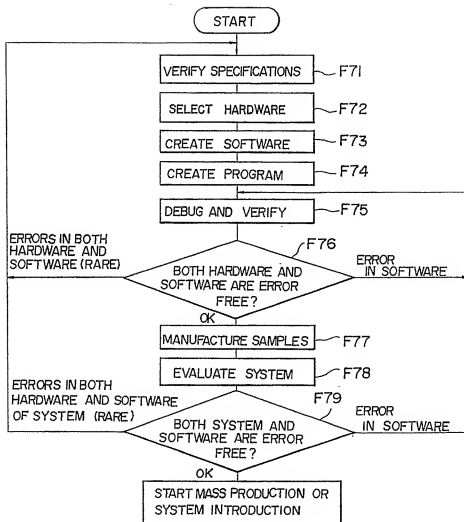


FIG.6

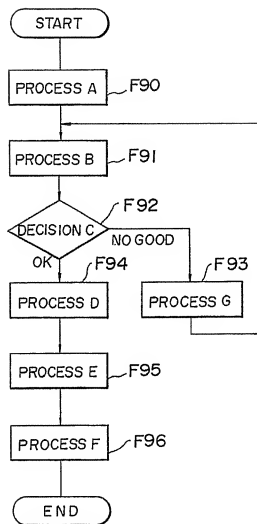


FIG.7